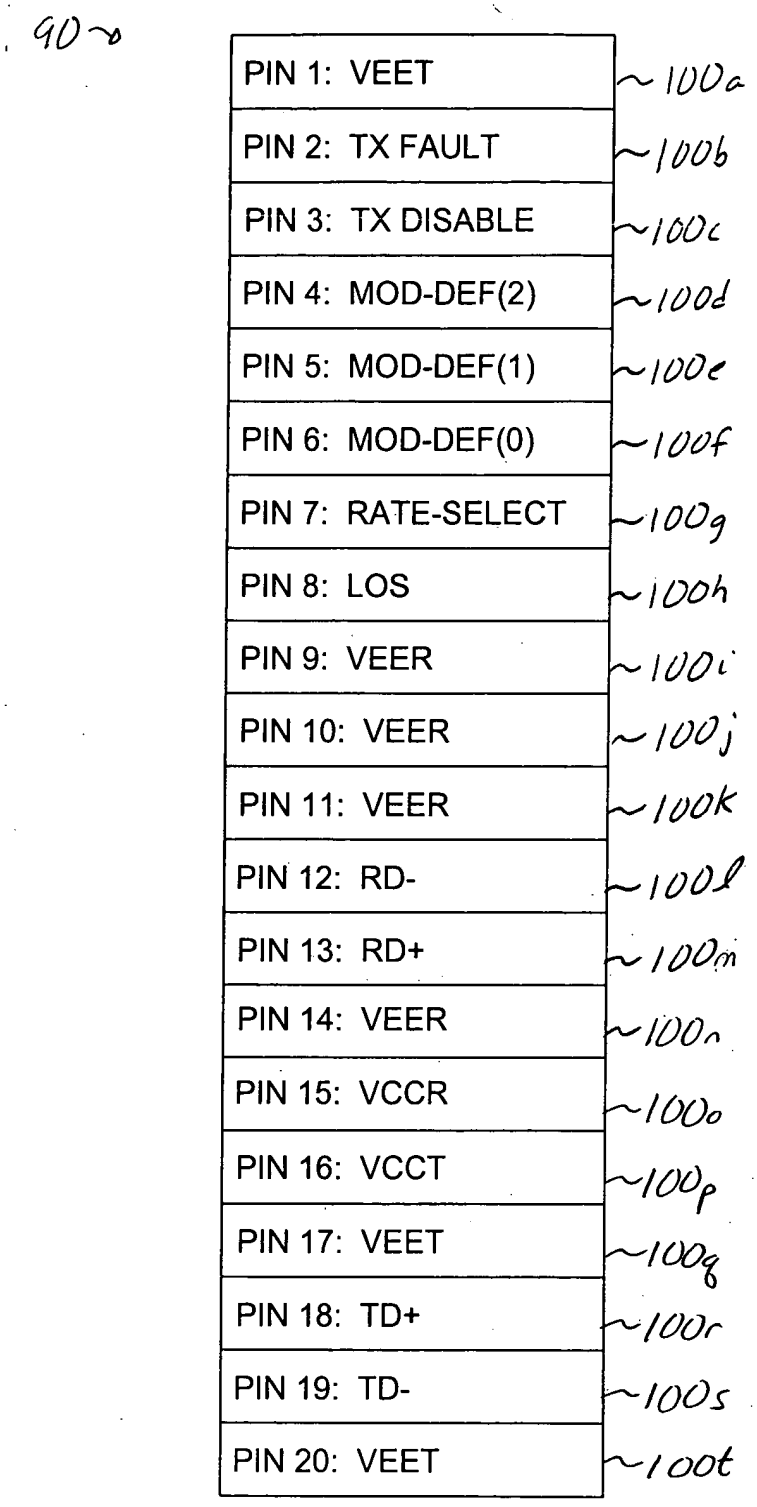
90
PIN 1: VEET
100a
PIN 2: TX FAULT
100b
PIN 3: TX DISABLE
100c
PIN 4: MOD-DEF(2)
100d
PIN 5: MOD-DEF(1)
100e
PIN 6: MOD-DEF(0)
100f
PIN 7: RATE-SELECT
100g
PIN 8: LOS
100h
PIN 9: VEER
100i
PIN 10: VEER
100j
PIN 11: VEER
100k
PIN 12: RD-
100l
PIN 13: RD+
100m
PIN 14: VEER
100n
PIN 15: VCCR
100o
PIN 16: VCCT
100p
PIN 17: VEET
100q
PIN 18: TD+
100r
PIN 19: TD-
100s
PIN 20: VEET
100t

Fig. 1

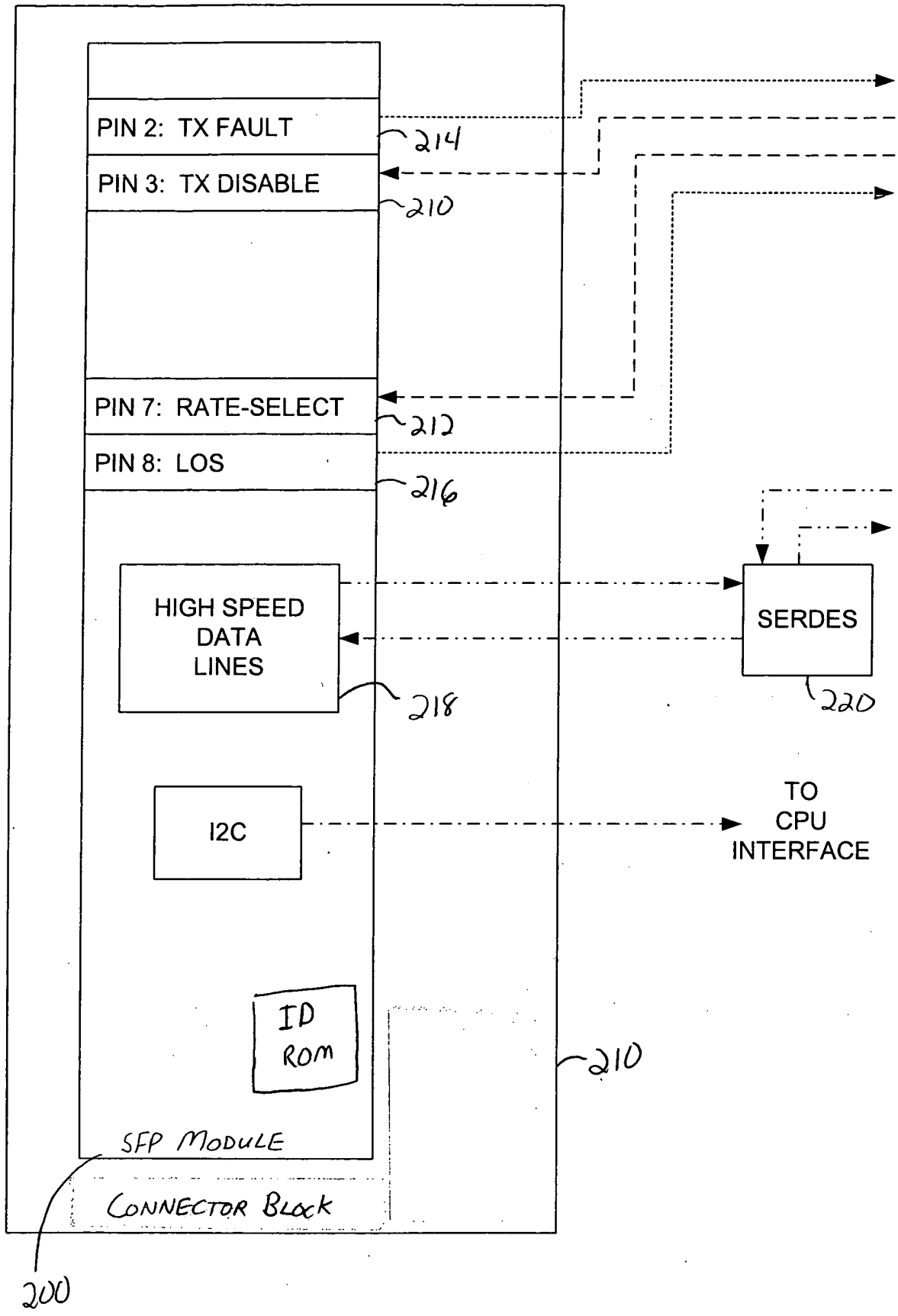
PIN 2: TX FAULT
214
PIN 3: TX DISABLE
210
PIN 7: RATE-SELECT
212
PIN 8: LOS
216
HIGH SPEED DATA LINES
218
SERDES
220
I2C
TO CPU INTERFACE
ID ROM
210
SFP MODULE
CONNECTOR BLOCK
200

Fig. 2

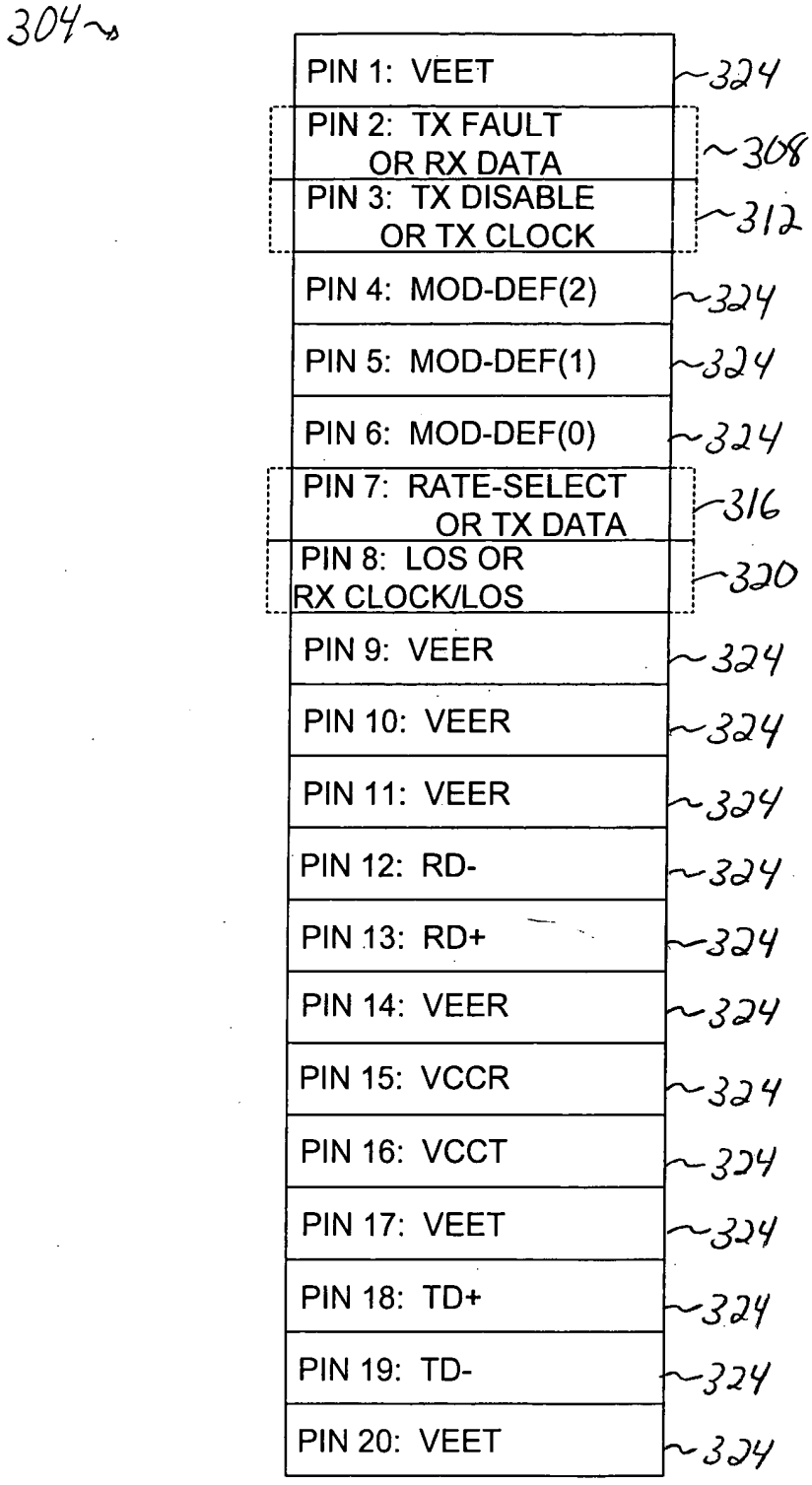
304
PIN 1: VEET
324
PIN 2: TX FAULT OR RX DATA
308
PIN 3: TX DISABLE OR TX CLOCK
312
PIN 4: MOD-DEF(2)
324
PIN 5: MOD-DEF(1)
324
PIN 6: MOD-DEF(0)
324
PIN 7: RATE-SELECT OR TX DATA
316
PIN 8: LOS OR RX CLOCK/LOS
320
PIN 9: VEER
324
PIN 10: VEER
324
PIN 11: VEER
324
PIN 12: RD-
324
PIN 13: RD+
324
PIN 14: VEER
324
PIN 15: VCCR
324
PIN 16: VCCT
324
PIN 17: VEET
324
PIN 18: TD+
324
PIN 19: TD-
324
PIN 20: VEET
324

Fig. 3

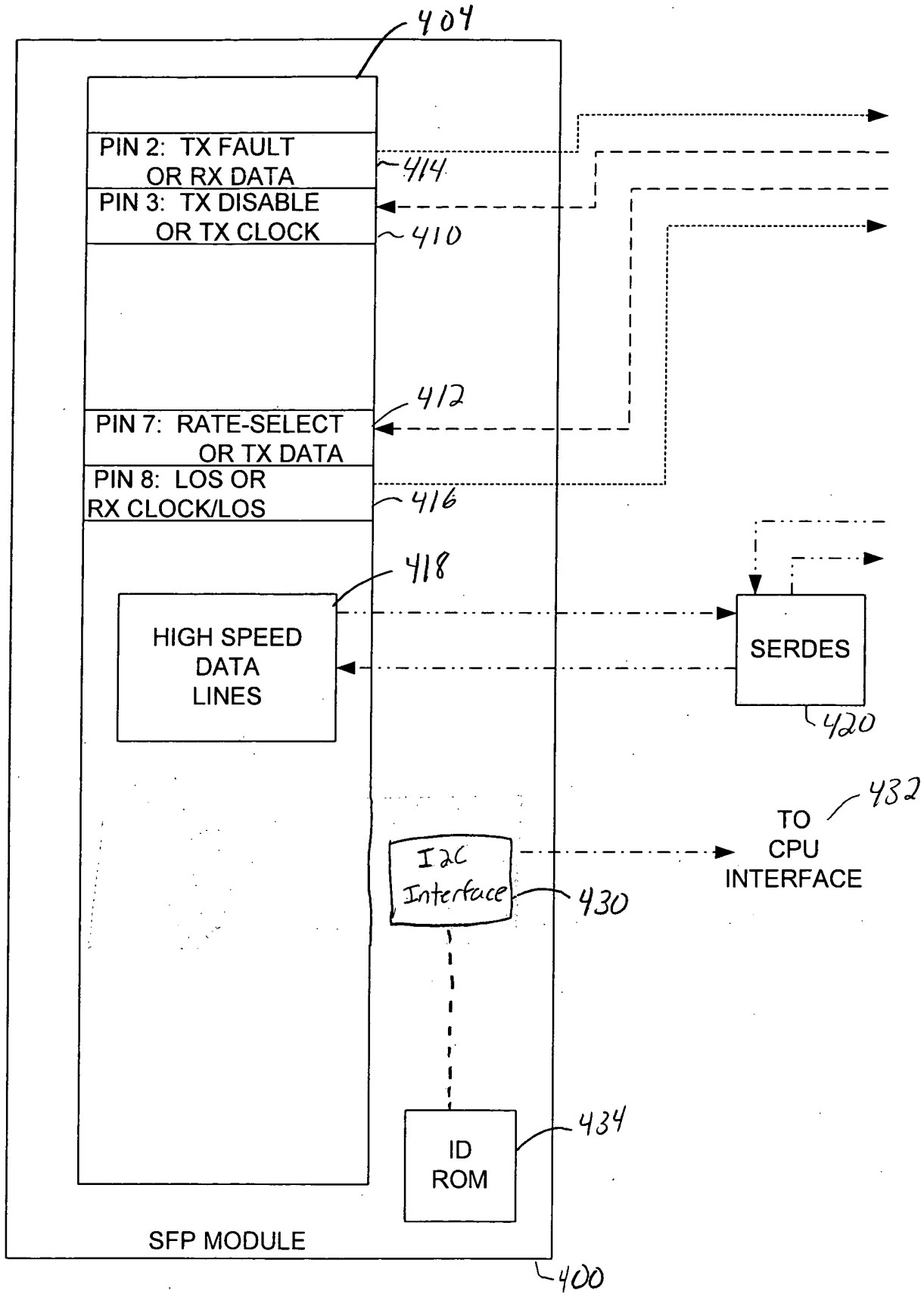
404
PIN 2: TX FAULT OR RX DATA
414
PIN 3: TX DISABLE OR TX CLOCK
410
412
PIN 7: RATE-SELECT OR TX DATA
PIN 8: LOS OR RX CLOCK/LOS
416
418
HIGH SPEED DATA LINES
SERDES
420
432
TO CPU INTERFACE
I2C Interface
430
ID ROM
434
SFP MODULE
400

Fig. 4

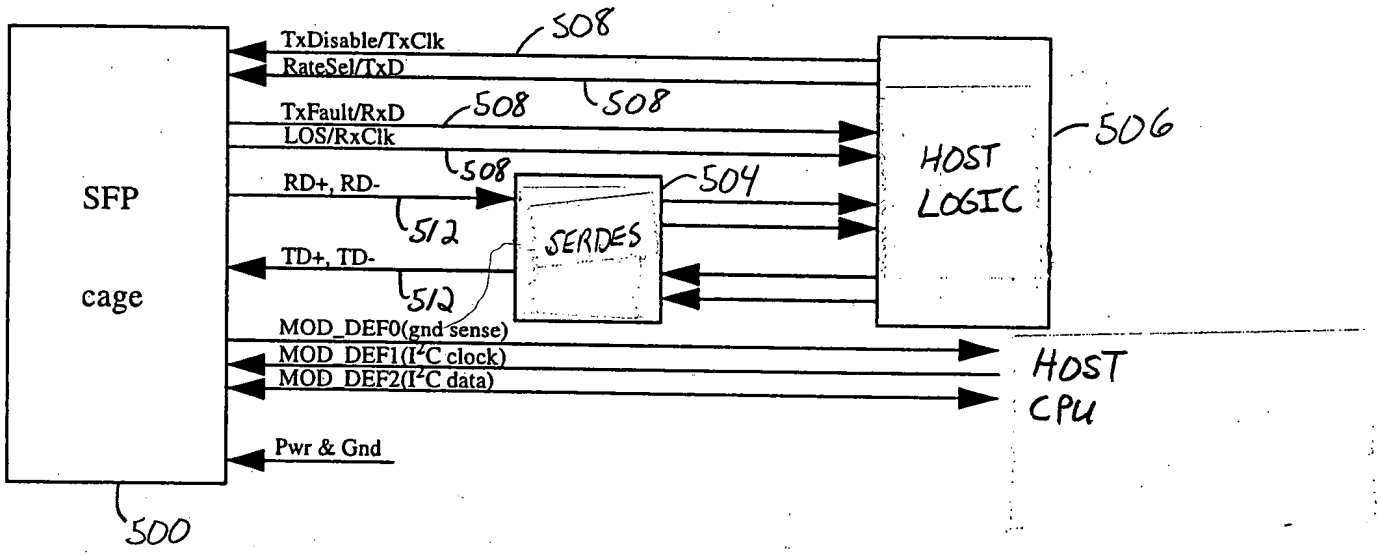
SFP
cage
500
TxDisable/TxClk
RateSel/TxD
TxFault/RxD
LOS/RxClk
RD+, RD-
TD+, TD-
MOD_DEF0(gnd sense)
MOD_DEF1(I²C clock)
MOD_DEF2(I²C data)
Pwr & Gnd
508
508
508
508
512
512
SERDES
504
HOST LOGIC
506
HOST CPU

Fig. 5

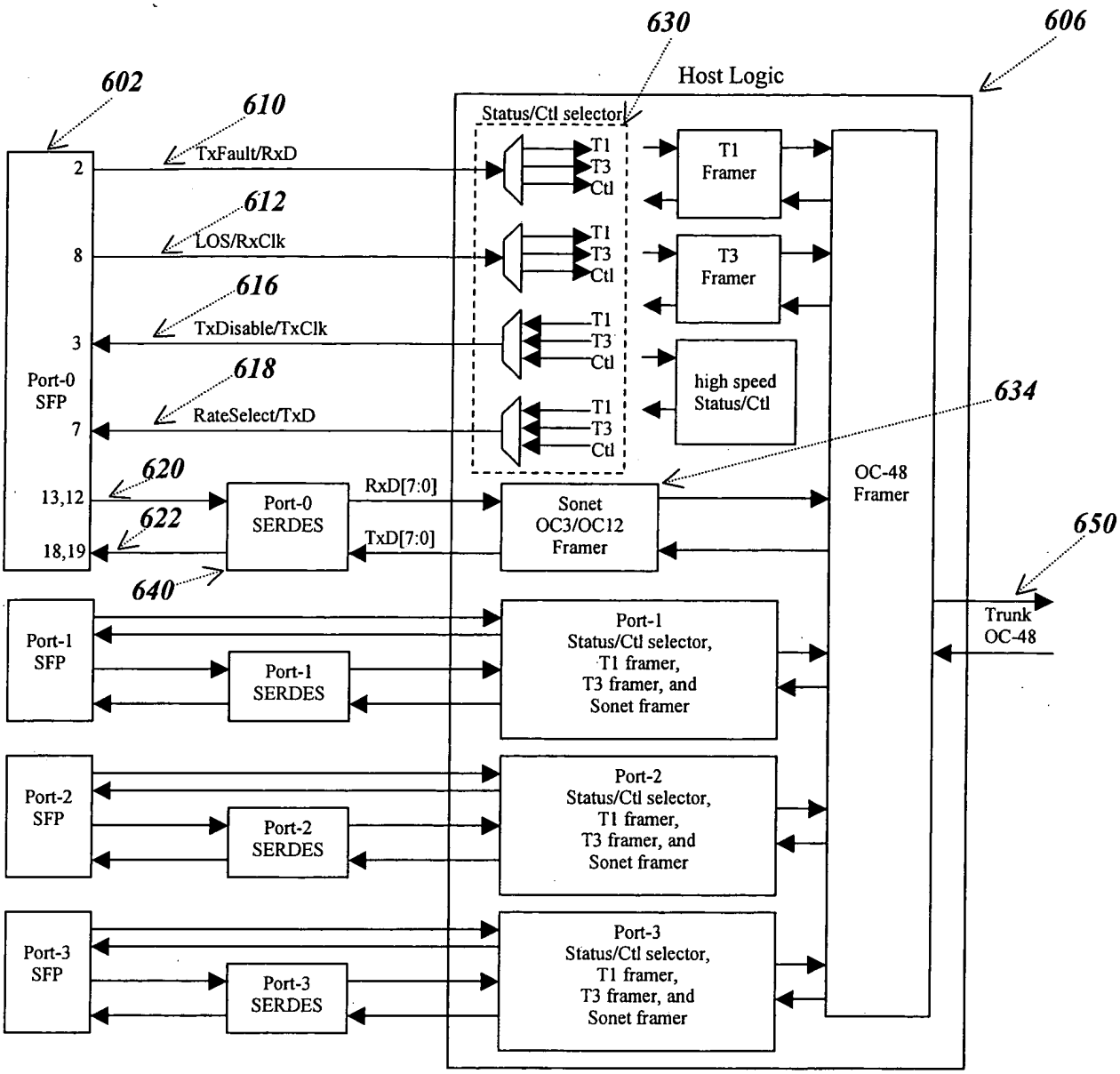
630
606
602
610
Host Logic
Status/Ctl selector
TxFault/RxD
2
T1
T3
Ctl
T1
Framer
612
LOS/RxClk
8
T3
Framer
616
TxDisable/TxClk
3
high speed
Status/Ctl
Port-0
SFP
618
RateSelect/TxD
7
634
620
13,12
Port-0
SERDES
RxD[7:0]
Sonet
OC3/OC12
Framer
OC-48
Framer
650
622
18,19
TxD[7:0]
640
Port-1
SFP
Port-1
SERDES
Port-1
Status/Ctl selector,
T1 framer,
T3 framer, and
Sonet framer
Trunk
OC-48
Port-2
SFP
Port-2
SERDES
Port-2
Status/Ctl selector,
T1 framer,
T3 framer, and
Sonet framer
Port-3
SFP
Port-3
SERDES
Port-3
Status/Ctl selector,
T1 framer,
T3 framer, and
Sonet framer

Fig. 6

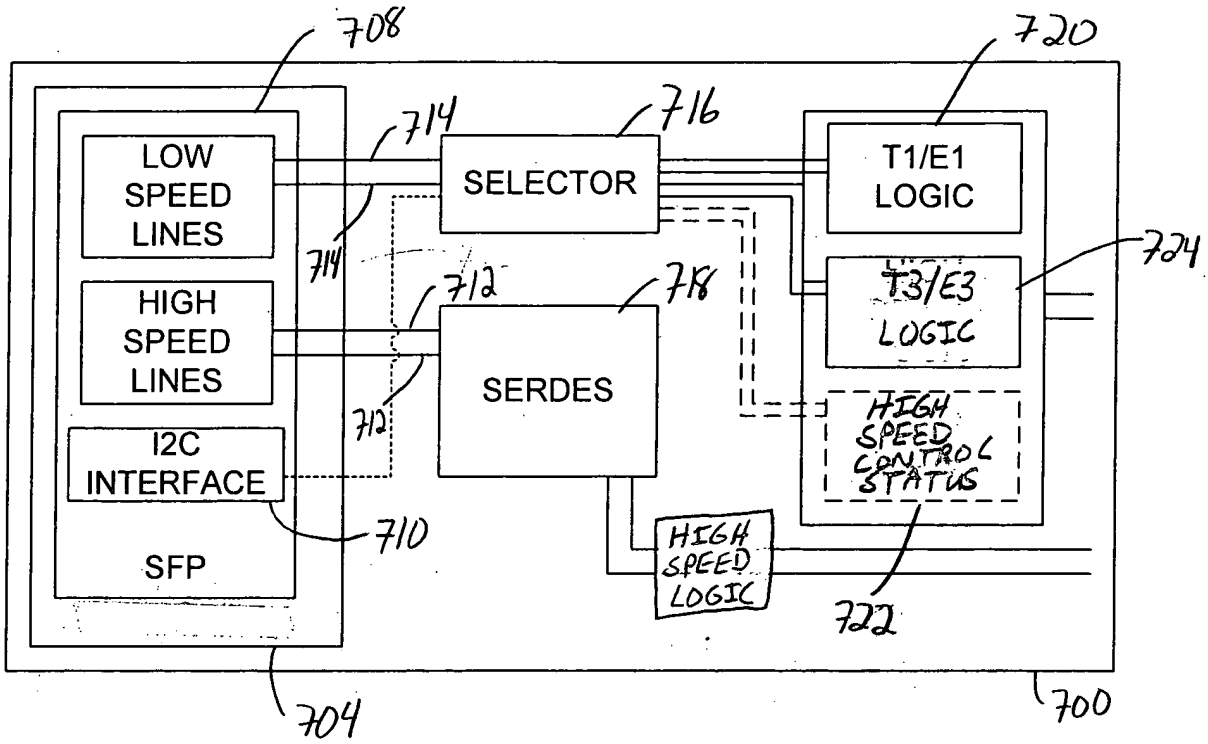
708
720
LOW SPEED LINES
714
716
SELECTOR
T1/E1 LOGIC
724
HIGH SPEED LINES
712
718
T3/E3 LOGIC
SERDES
712
HIGH SPEED CONTROL STATUS
I2C INTERFACE
710
HIGH SPEED LOGIC
722
SFP
704
700

Fig. 7

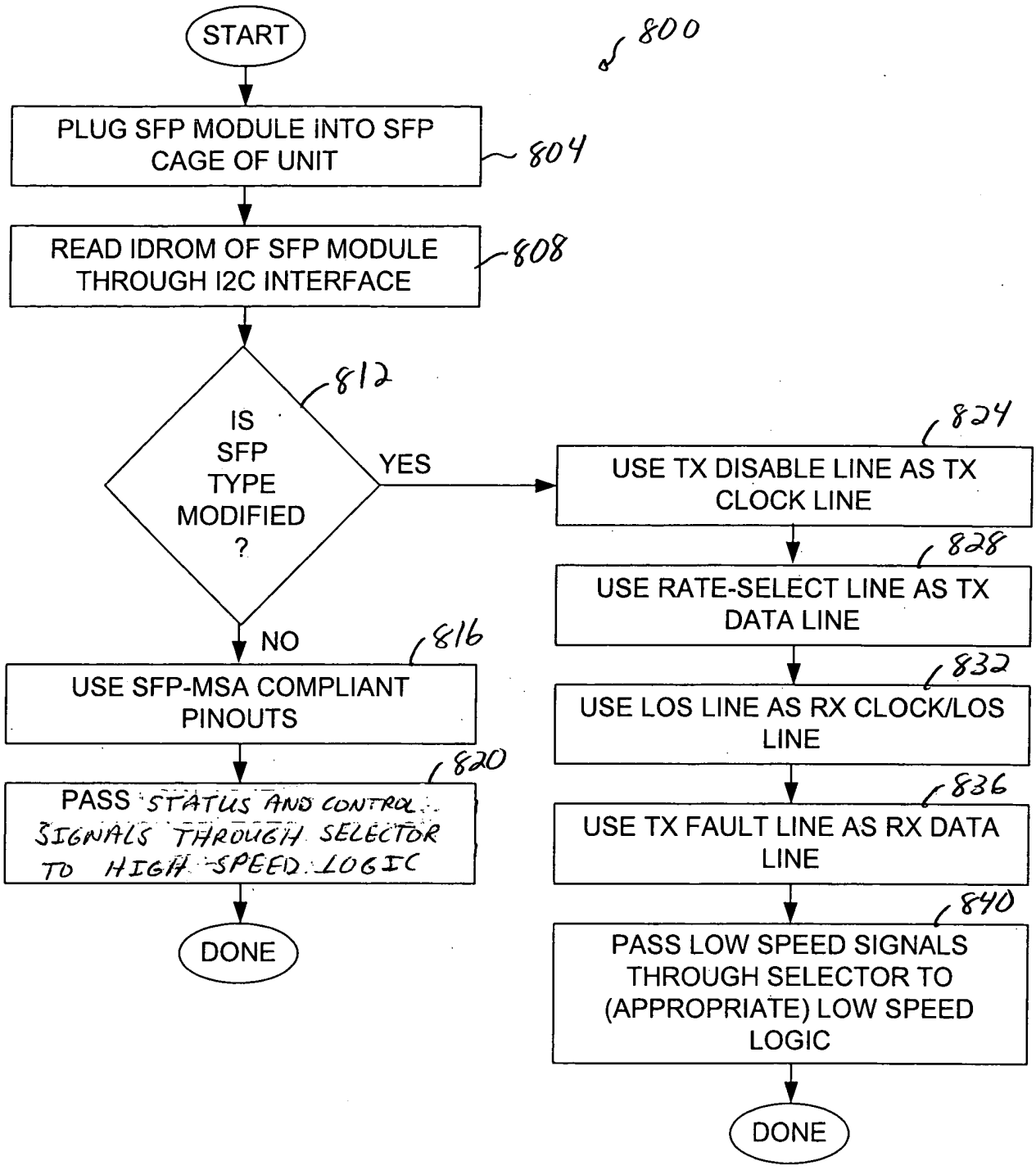
800
START
PLUG SFP MODULE INTO SFP CAGE OF UNIT
804
READ IDROM OF SFP MODULE THROUGH I2C INTERFACE
808
IS SFP TYPE MODIFIED ?
812
YES
NO
USE TX DISABLE LINE AS TX CLOCK LINE
824
USE RATE-SELECT LINE AS TX DATA LINE
828
USE LOS LINE AS RX CLOCK/LOS LINE
832
USE TX FAULT LINE AS RX DATA LINE
836
PASS LOW SPEED SIGNALS THROUGH SELECTOR TO (APPROPRIATE) LOW SPEED LOGIC
840
DONE
USE SFP-MSA COMPLIANT PINOUTS
816
PASS STATUS AND CONTROL SIGNALS THROUGH SELECTOR TO HIGH SPEED LOGIC
820
DONE

Fig. 8

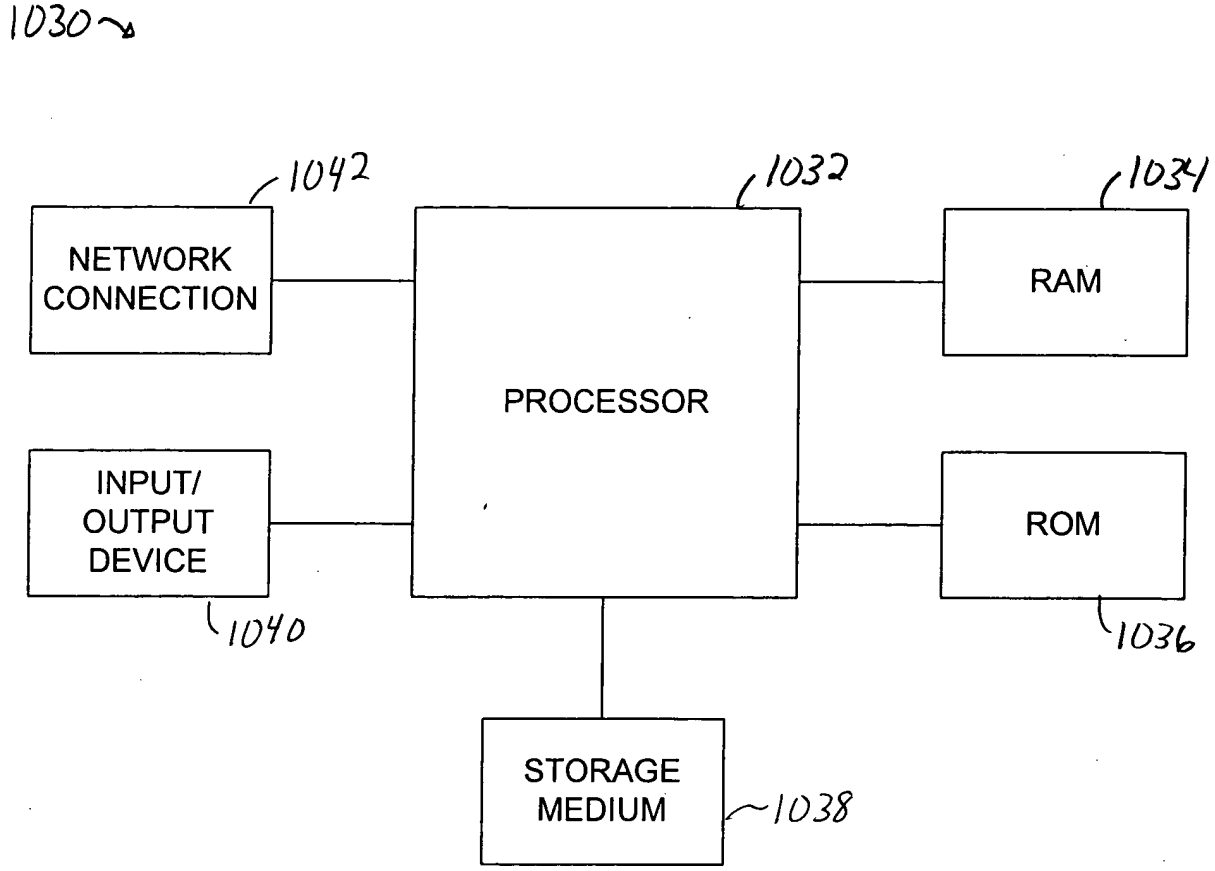
1030
1042
1032
1034
NETWORK CONNECTION
PROCESSOR
RAM
INPUT/ OUTPUT DEVICE
ROM
1040
1036
STORAGE MEDIUM
1038

Fig. 9